



PRODUCT SPECIFICATION

- Tentative Specification
- Preliminary Specification
- Approval Specification

**MODEL NO.: V370H4
SUFFIX: LE2**

Customer:**APPROVED BY****SIGNATURE**Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

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CONTENTS

1. GENERAL DESCRIPTION.....	5
1.1 OVERVIEW.....	5
1.2 FEATURES.....	5
1.3 APPLICATION.....	5
1.4 GENERAL SPECIFICATIONS	5
1.5 MECHANICAL SPECIFICATION.....	6
2. ABSOLUTE MAXIMUM RATINGS.....	7
2.1 ABSOLUTE RATINGS OF ENVIRONMENT.....	7
2.2 PACKAGE STORAGE	8
2.3 ELECTRICAL ABSOLUTE RATINGS.....	8
2.3.1 TFT LCD MODULE.....	8
2.3.2 BACKLIGHT CONVERTER UNIT	8
3. ELECTRICAL CHARACTERISTICS	9
3.1 TFT LCD MODULE.....	9
3.2 BACKLIGHT UNIT.....	12
3.2.1 LED CHARACTERISTICS ($T_a=25\pm 2$ °C).....	12
3.2.2 CONVERTER CHARACTERISTICS	12
3.2.3 CONVERTER INTERFACE CHARACTERISTICS.....	13
4. BLOCK DIAGRAM OF INTERFACE	15
4.1 TFT LCD MODULE.....	15
5. INPUT TERMINAL PIN ASSIGNMENT	16
5.1 TFT LCD Module Input CNF1 Connector Pin Assignment (GS13512-1411S-7F(Foxconn)).....	16
5.3 CONVERTER UNIT.....	18
5.4 BLOCK DIAGRAM OF INTERFACE	19
5.5 LVDS INTERFACE	20
5.6 COLOR DATA INPUT ASSIGNMENT.....	22
6. INTERFACE TIMING.....	23
6.1 INPUT SIGNAL TIMING SPECIFICATIONS.....	23
6.2 POWER ON/OFF SEQUENCE	26
7. OPTICAL CHARACTERISTICS	27
7.1 TEST CONDITIONS.....	27

7.2 OPTICAL SPECIFICATIONS	28
8. PRECAUTIONS	31
8.1 ASSEMBLY AND HANDLING PRECAUTIONS	31
8.2 SAFETY PRECAUTIONS	31
9. DEFINITION OF LABELS.....	32
9.1 CMO MODULE LABEL.....	32
10. PACKAGING	33
10.1 PACKING SPECIFICATIONS.....	33
10.2 PACKING METHOD	33
11. MECHANICAL CHARACTERISTICS	35



PRODUCT SPECIFICATION

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 0.0	May. 26. 2010	All	All	The Preliminary Specification was first issued.



PRODUCT SPECIFICATION

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V370H4-LE2 is a 37" TFT Liquid Crystal Display module with LED Backlight and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display true 16.7M colors (8bit). The converter module for backlight is built-in.

1.2 FEATURES

- High brightness (450 nits)
- High contrast ratio (6000:1)
- Fast response time (Gray to gray average 6.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60Hz or 50Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	819.36 (H) x 460.89 (V) (37" diagonal)	mm	(1)
Bezel Opening Area	826.4(H) x 468 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.14225 (H) x 0.42675 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally Black	-	
Surface Treatment	Anti-Glare Coating (Haze 11%) Hard Coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.



PRODUCT SPECIFICATION

1.5 MECHANICAL SPECIFICATION

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	861.2	862.4	863.6	mm
	Vertical(V)	502.8	504	505.2	mm
	Depth(D)	14	15.2	16.4	mm To rear
	Depth(D)	24.4	25.6	26.8	mm To converter cover
Weight		6185		g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	X, Y axis	-	50	G (3), (5)
		Z axis	-	35	G (3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

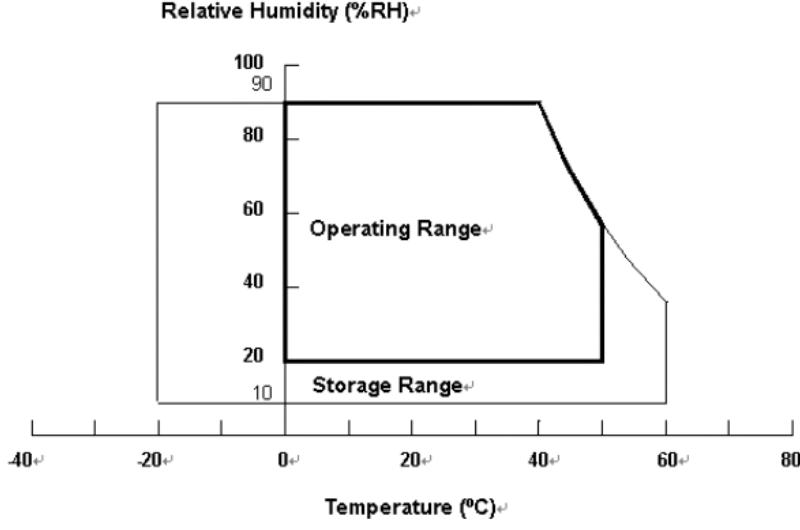
- (a) 90 %RH Max. ($T_a \leq 40$ °C).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.





PRODUCT SPECIFICATION

2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Light Bar Voltage	VW	—	60	VRMS	
Converter Input Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, Internal PWM Control and External PWM Control.

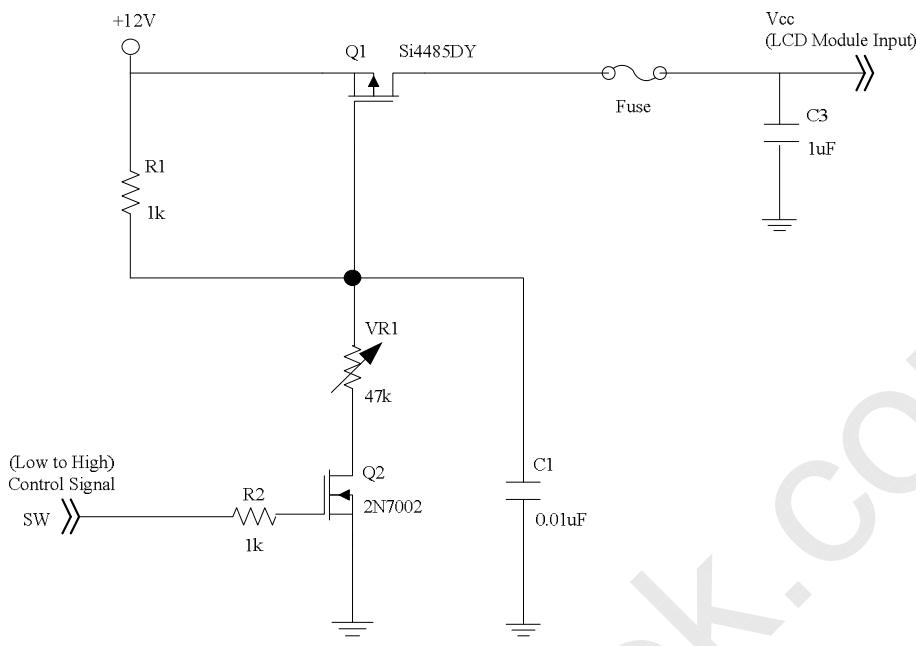
3. ELECTRICAL CHARACTERISTICS**3.1 TFT LCD MODULE**

(Ta = 25 ± 2 °C)

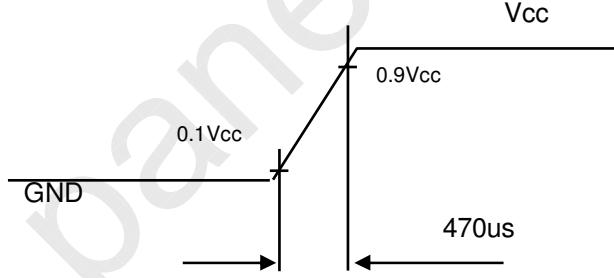
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V _{CC}	10.8	12	13.2	V	(1)
Rush Current	I _{RUSH}	-	-	2.8	A	(2)
Power Supply Current	White Pattern	-	-	0.32	-	A
	Horizontal Stripe	-	-	0.55	0.66	A
	Black Pattern	-	-	0.31	-	A
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	-	-	mV
	Differential Input Low Threshold Voltage	V _{LVTL}	-	-	-100	mV
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V
	Differential input voltage (Single-end)	V _{ID}	200	-	600	mV
	Terminating Resistor	R _T	-	100	-	ohm
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



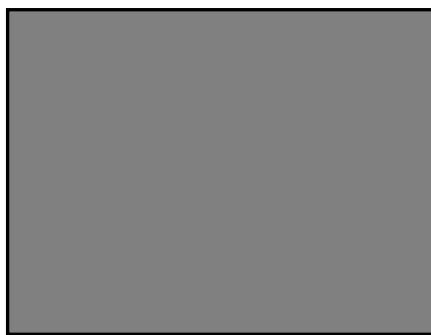
Note (3) The specified power supply current is under the conditions at $V_{CC} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



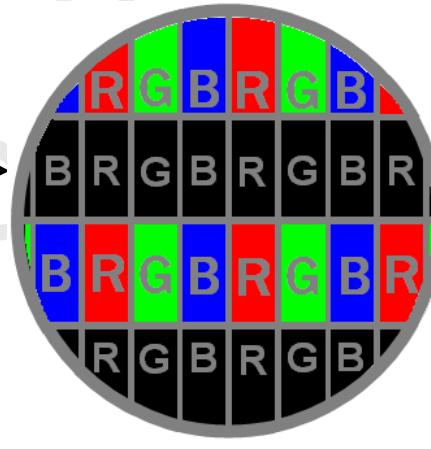
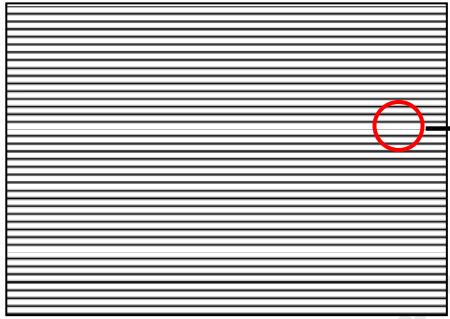
Active Area

b. Black Pattern

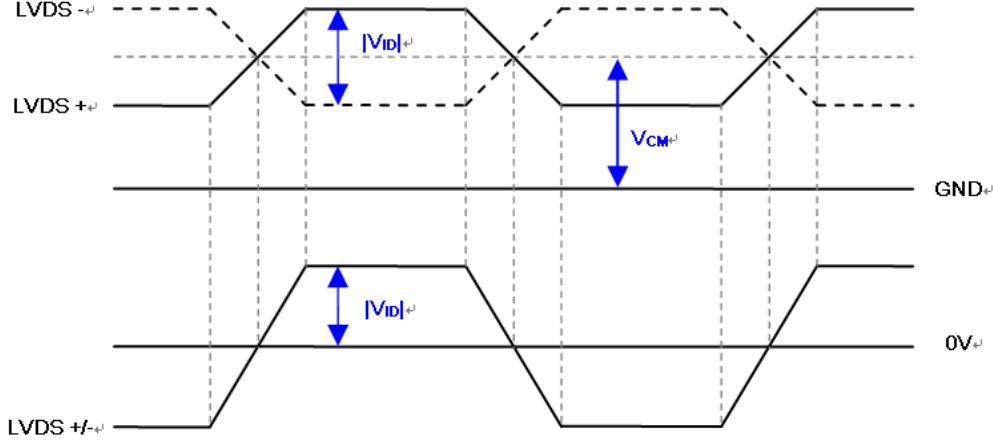


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN2, 4 : 161035-10041-3 (P-TWO) or 7083K-F10N-04L(E&T) or equivalent

Pin №	Symbol	Feature	NOTE
1	VLED	Positive of LED String	
2	VLED		
3	NC	No Connection	
4	NC		
5	NC		
6	NC		
7	N1	Negative of LED String	
8	N2		
9	N3		
10	N4		

Note (1) The backlight interface housing for high voltage side is a model 161035-10041-3, manufactured by P-TWO or equivalent.

3.2.1 LED CHARACTERISTICS (Ta=25± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Forward Voltage	V _W	3.0		3.5	V _{RMS}	I _L = 120.0mA
LED Current	I _L	-	120		mA _{RMS}	

3.2.2 CONVERTER CHARACTERISTICS

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	TBD	TBD	W	IL = 80mA
Power Supply Voltage	V _{BL}	22.8	24.0	25.2	VDC	
Power Supply Current	I _{BL}	-	TBD	TBD	A	Non Dimming
Dimming Frequency	F _B	150	160	170	Hz	
Minimum Duty Ratio	D _{MIN}	5	10	-	%	(1)

Note (1) 5% minimum duty ratio is only valid for electrical operation.

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

External dimming: 150Hz~170Hz, duty ratio: 10%~100%

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	3.15	—	3.45	V	maximum duty ratio
	MIN		—	—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO		—	0	—	0.8	V	Abnormal
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V _{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		TPWMR	—	—	—	50	us	
PWM Signal Falling Time		TPWMF	—	—	—	50	us	
Input Impedance		Rin	—	1	—	—	MΩ	
PWM Delay Time		TPWM	—	100	—	—	ms	
BLON Delay Time	T _{on}	—	300	—	—	—	ms	
	T _{on1}	—	300	—	—	—	ms	
BLON Off Time		Toff	—	300	—	—	ms	

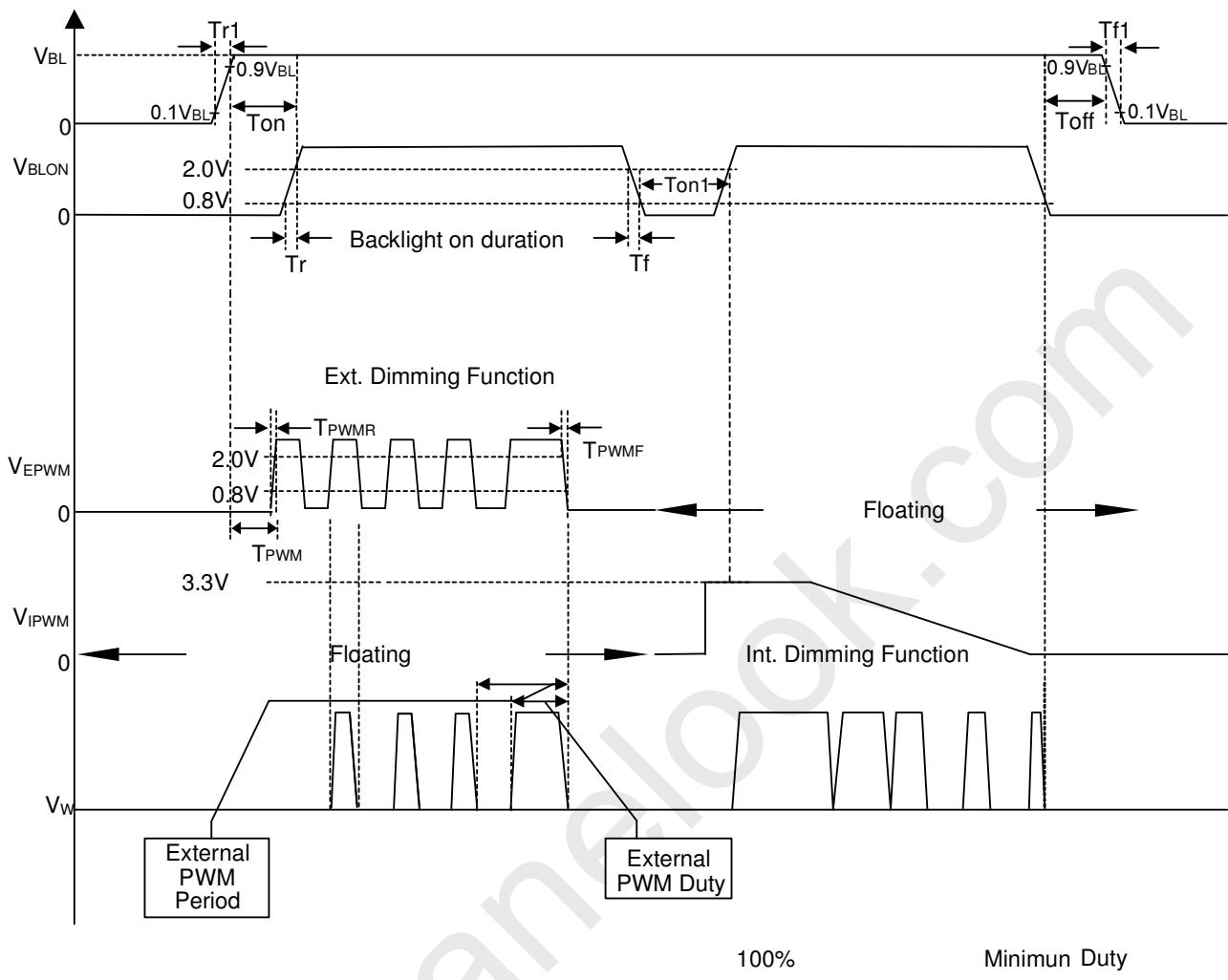
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

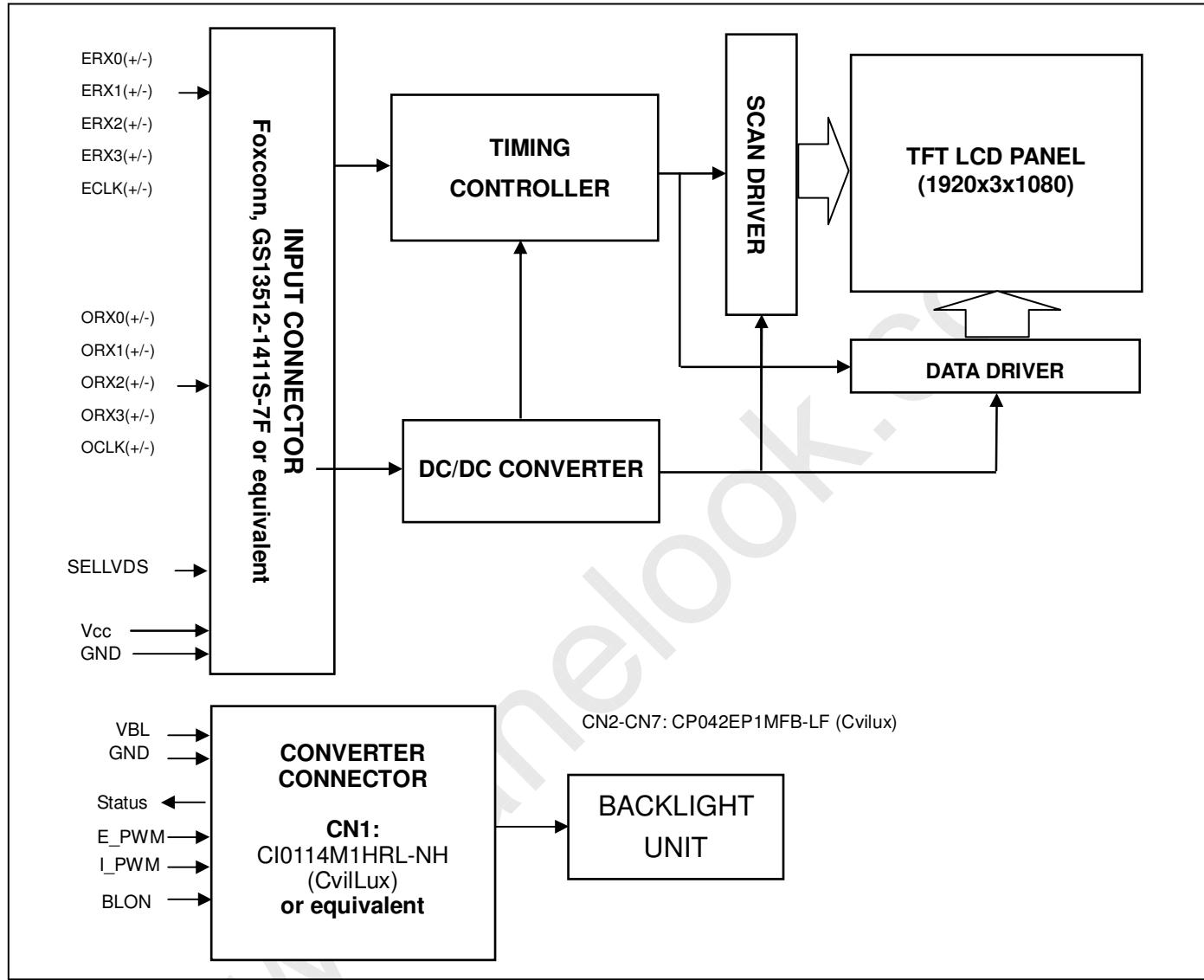
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

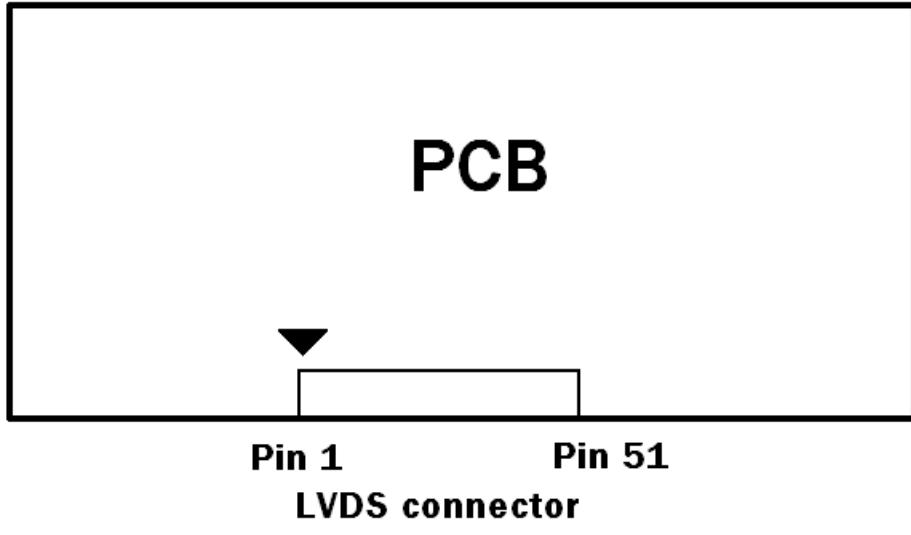
4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT**5.1 TFT LCD Module Input CNF1 Connector Pin Assignment (GS13512-1411S-7F(Foxconn))**

Pin	Name	Description	Note
1	GND	Ground	(2)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(3)(4)
8	N.C.	No Connection	(2)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input	(5)
20	ECLK+	Even pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(2)
25	N.C.	No Connection	
26	GND	Ground	
27	GND	Ground	
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	Odd pixel Negative LVDS differential clock input.	(5)
36	OCLK+	Odd pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(2)
41	N.C.	No Connection	
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) LVDS connector pin orderdefined as follows

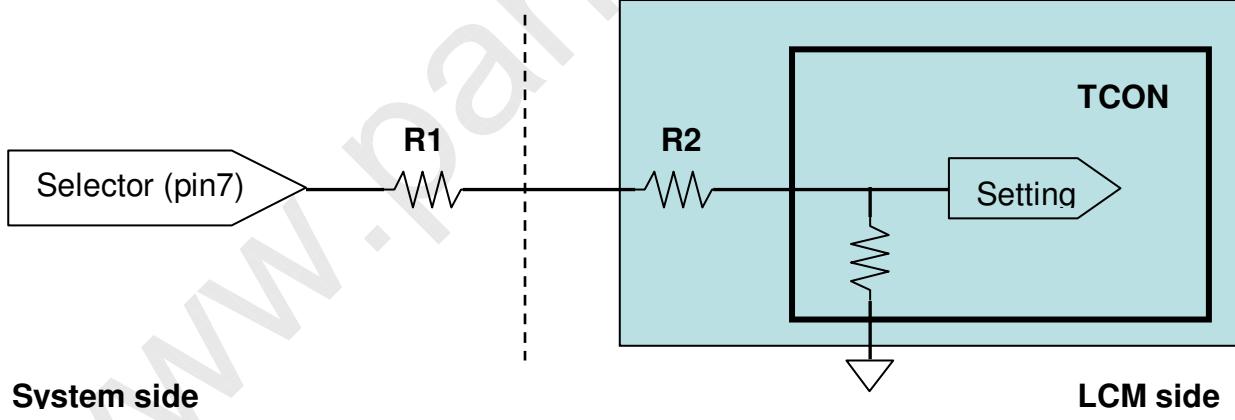


Note (2) Reserved for internal use. Please leave it open.

Note (3) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

Note (4) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ($R1 < 1K \text{ Ohm}$)



System side: $R1 < 1K$

Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.3 CONVERTER UNIT

CN1: CI0114M1HRL-NH (CvILux) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal(GND)
12	E_PWM	External PWM Control Signal
13	I_PWM	Internal PWM Control Signal
14	BLON	BL ON/OFF

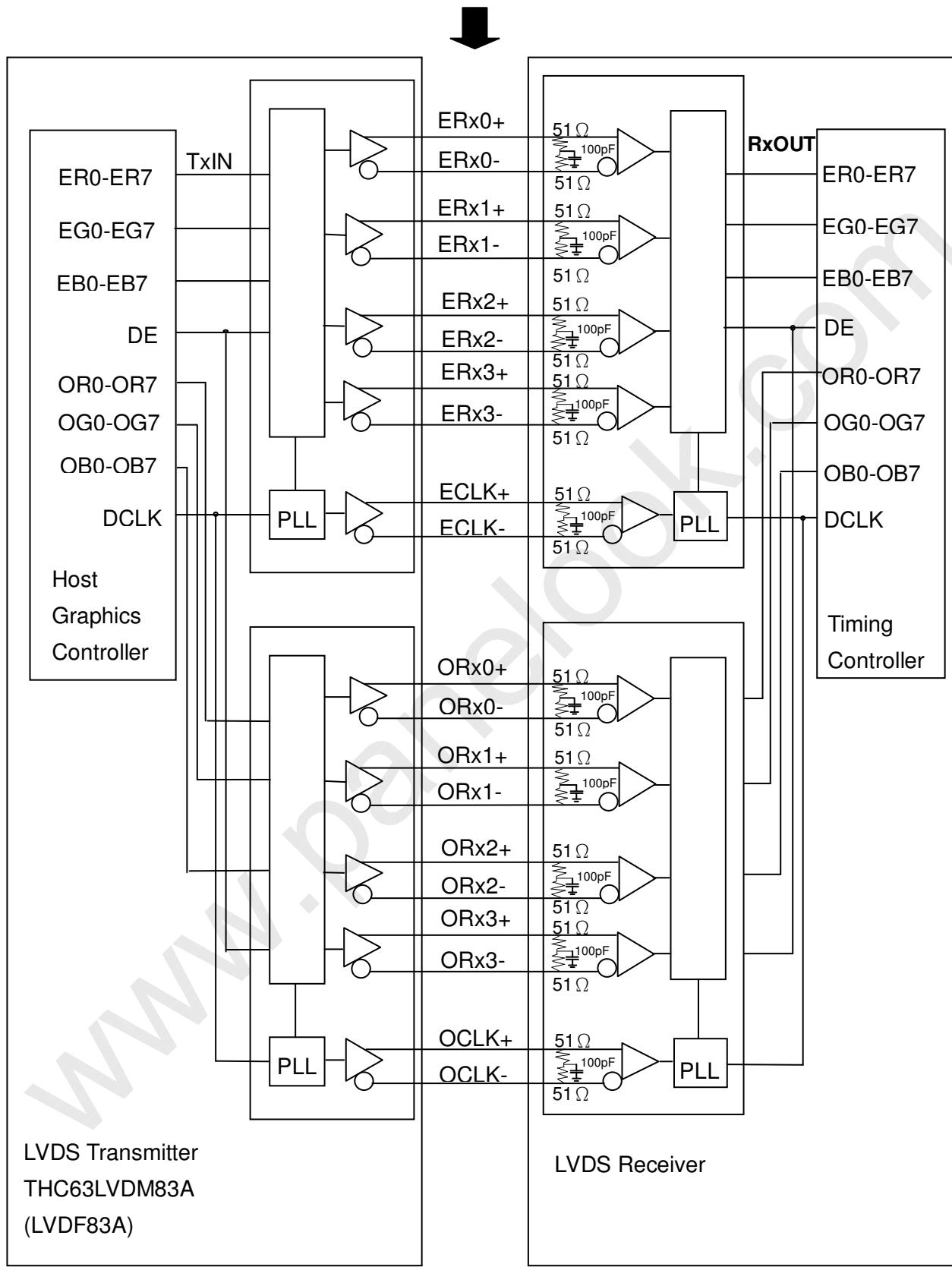
Note (1) Pin 12: External PWM control (use pin 12): Pin 13 must open.

Note (2) Pin 13: Internal PWM control (use pin 13): Pin 12 must open.

Note (3) Pin 12 and Pin 13 can't open in the same period.

CN2, 4 : 161035-10041-3 (P-TWO) or 7083K-F10N-04L(E&T) or equivalent

Pin №	Symbol	Feature	NOTE
1	N4	Negative of LED String	
2	N3		
3	N2		
4	N1		
5	NC	No Connection	
6	NC		
7	NC		
8	NC		
9	VLED	Positive of LED String	
10	VLED		

5.4 BLOCK DIAGRAM OF INTERFACE

ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

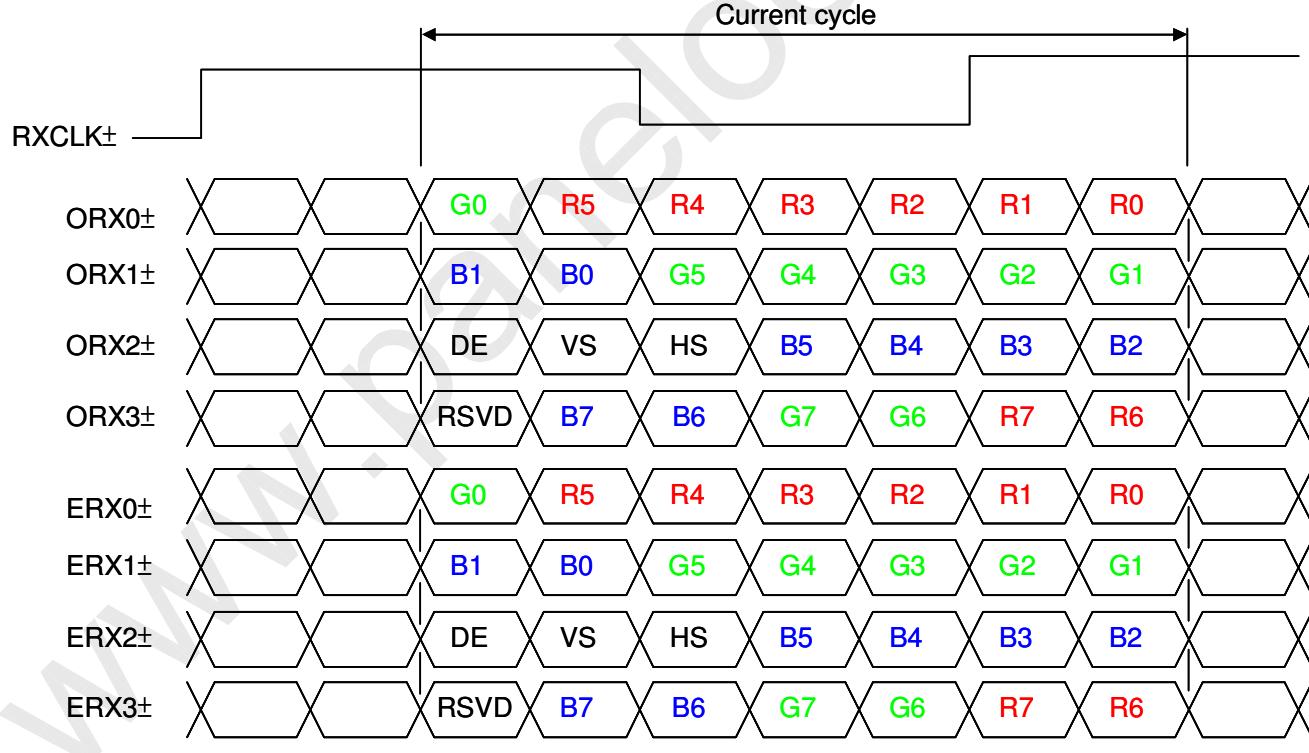
DCLK: Data clock signal

Notes (1) The system must have the transmitter to drive the module.

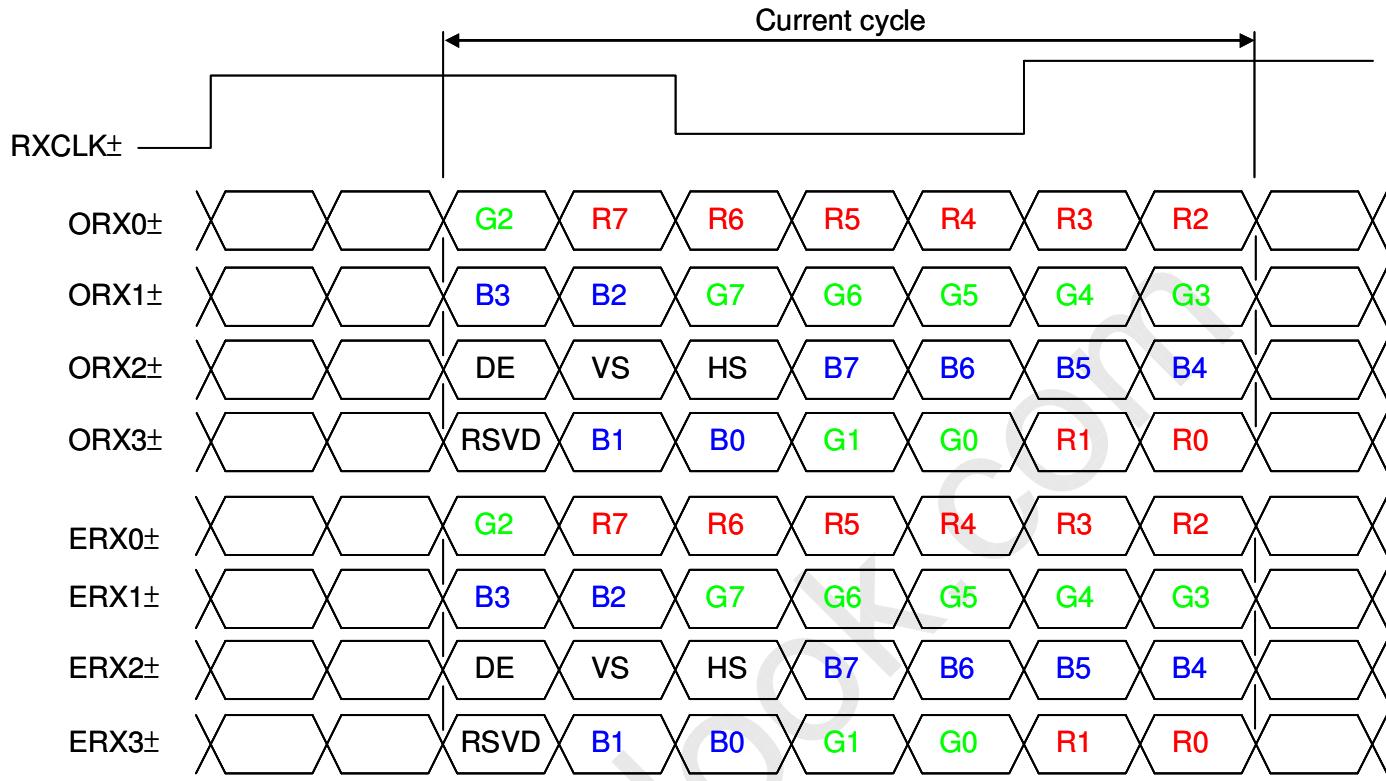
Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially

5.5 LVDS INTERFACE

VESA LVDS format : (SELLVDS pin=L or open)



JEDIA LVDS format : (SELLVDS pin=H)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color.

The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red (253)	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (253)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray Scale Of Blue	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F _{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T _{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F _{clkin_mod}	F _{clkin} -2%	—	F _{clkin} +2%	MHz	(4)
	Spread spectrum modulation frequency	F _{ssm}			200	KHz	
LVDS Receiver Data	Setup Time	T _{lvsu}	600	—	—	ps	(5)
	Hold Time	T _{lvhd}	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F _{r5}	47	50	53	Hz	(6)
		F _{r6}	57	60	63	Hz	
	Total	T _v	1115	1125	1135	Th	T _v =T _{vd} +T _{vb}
	Display	T _{vd}	1080	1080	1080	Th	—
	Blank	T _{vb}	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	1050	1100	1150	T _c	Th=Thd+Thb
	Display	Thd	960	960	960	T _c	—
	Blank	Thb	90	140	190	T _c	—

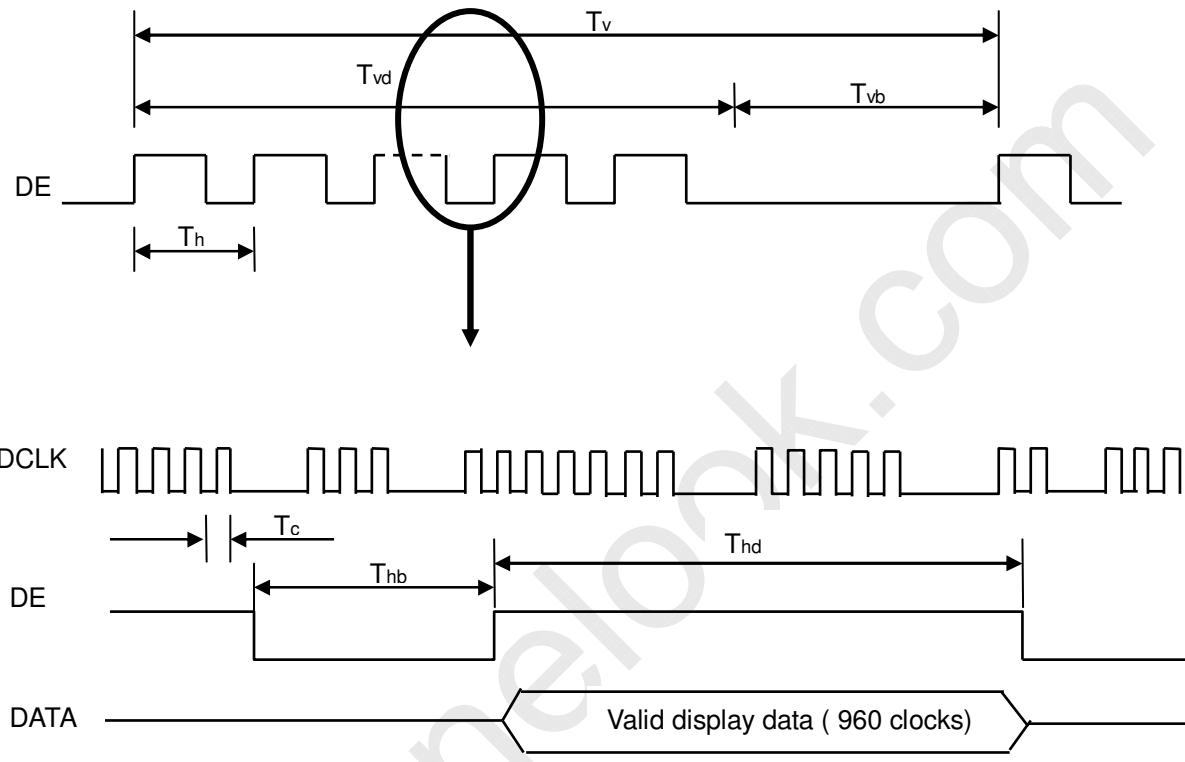
Note (1) Please make sure the range of pixel clock has follow the below equation :

$$F_{clkin}(\max) \geq F_{r6} \times T_v \times Th$$

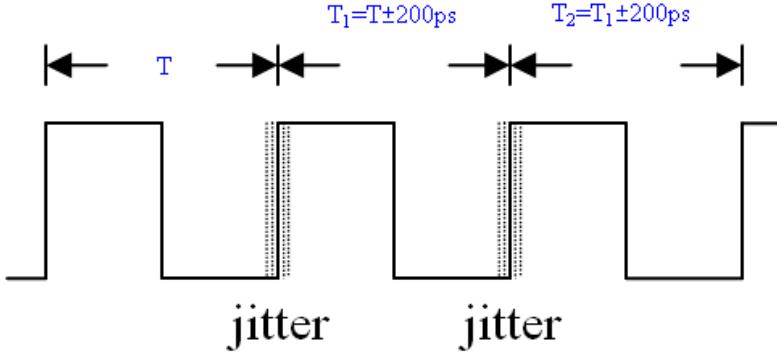
$$Fr5 \times T_v \times Th \geq F_{clkin}(\min)$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

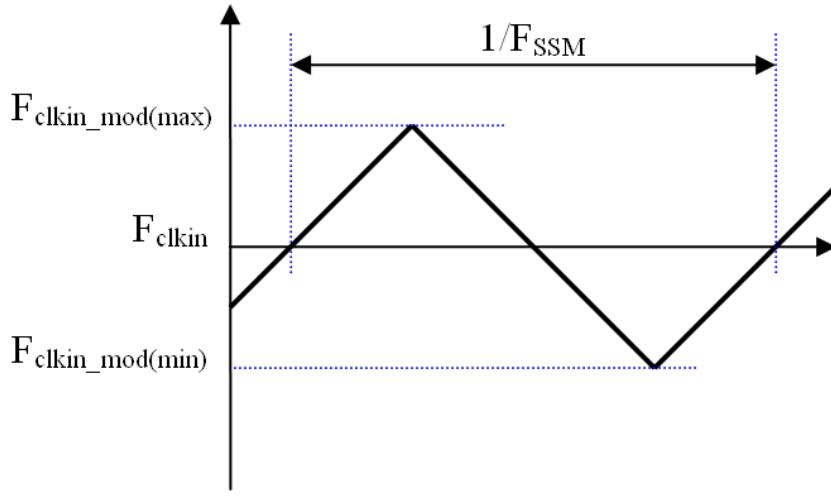
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_2|$

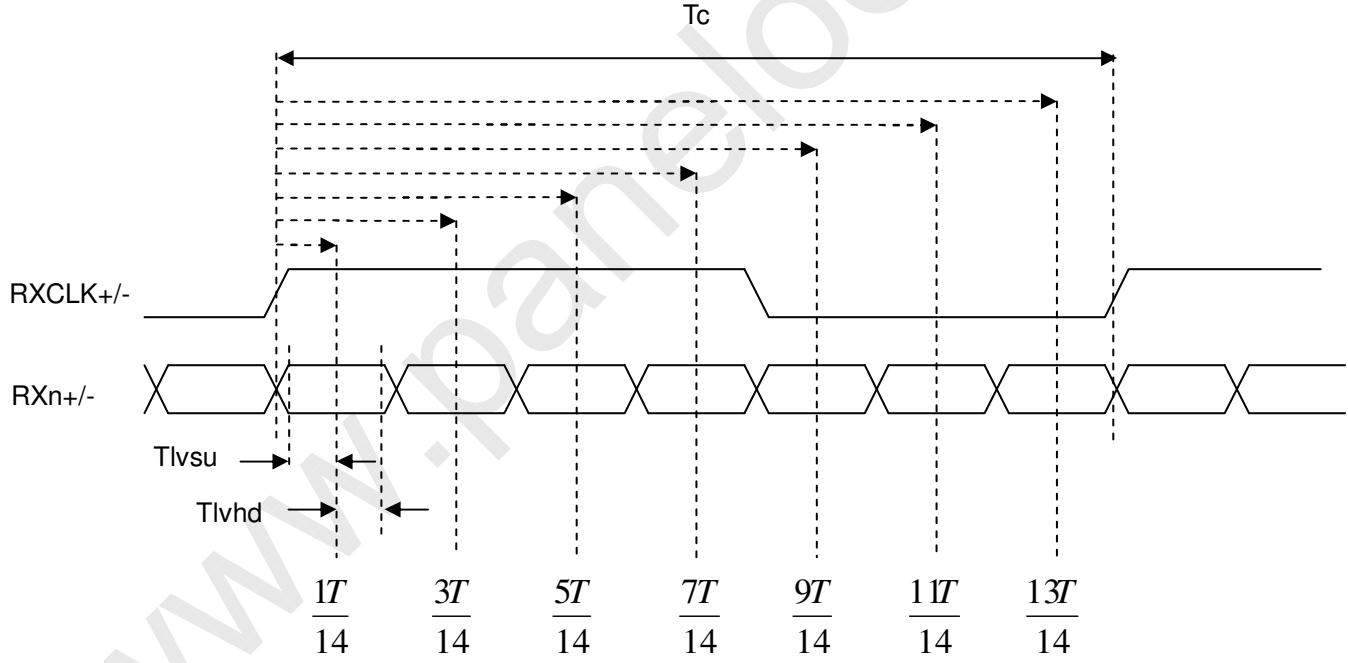


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

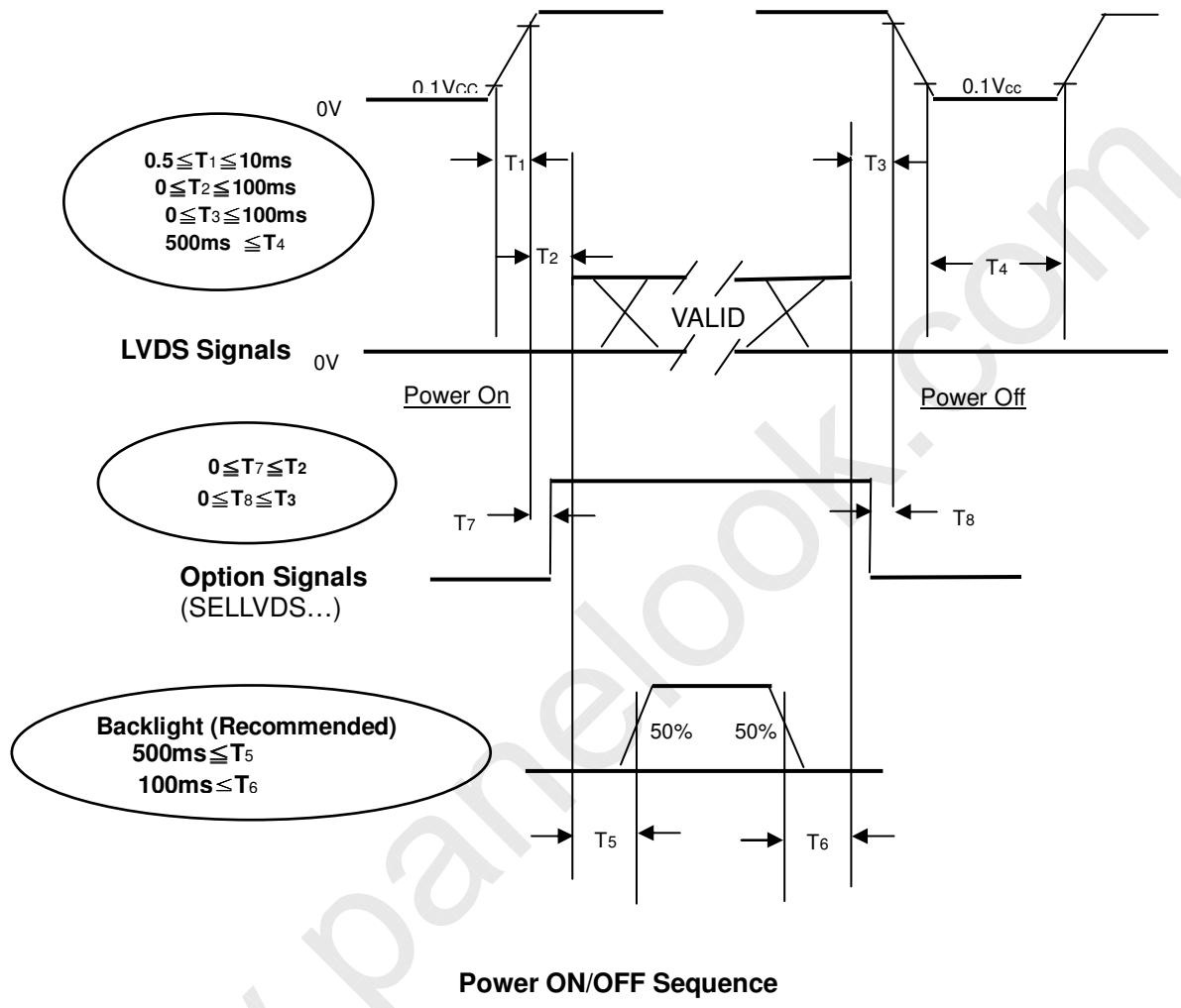


Note (6) : (ODSEL) = H/L or open for 50/ 60Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 °C)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



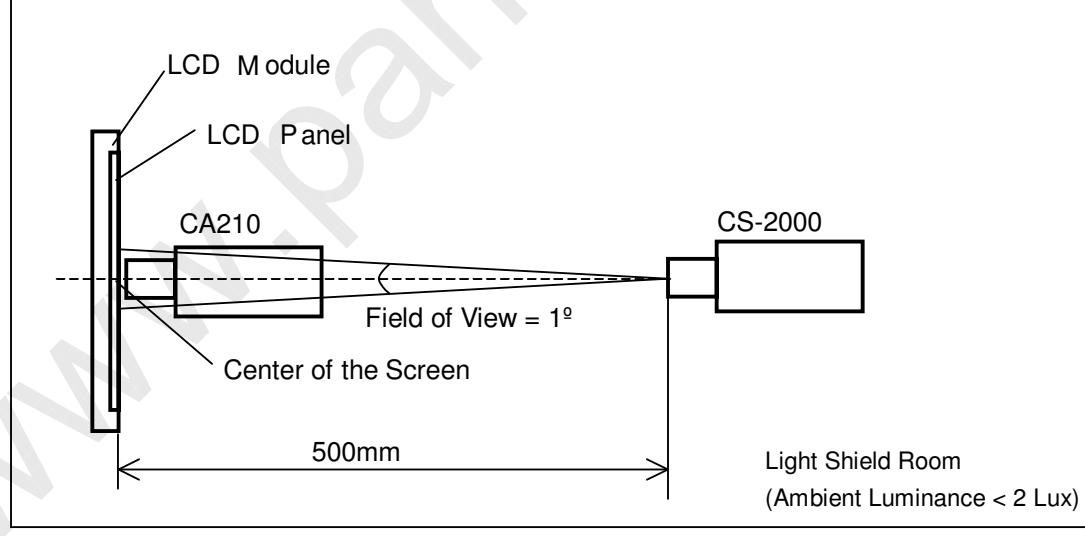
Note.

- (1) The supply voltage of the external system for the module input should follow the definition of Vcc.
- (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failures.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS**7.1 TEST CONDITIONS**

Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	(120 ±3.6)	mA
Vertical Frame Rate	F _r	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



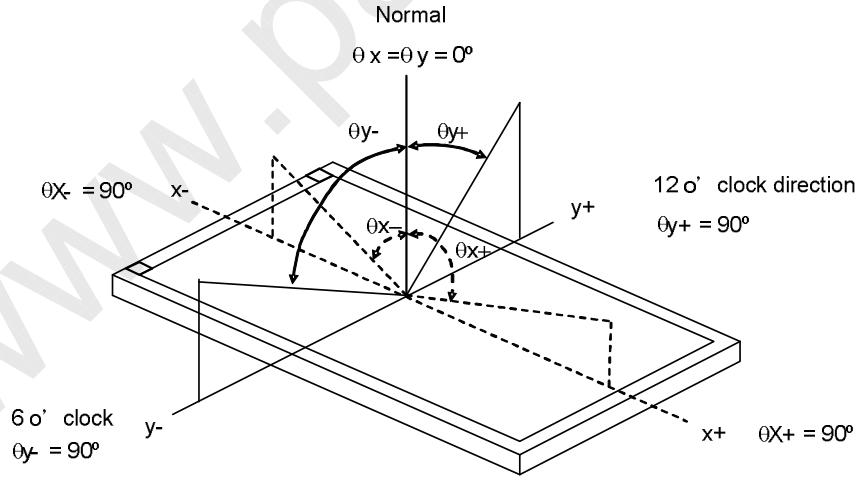
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio	CR		(4200)	(6000)	-	-	Note (2)	
Response Time	Gray to gray		-	(5.0)	-	ms	Note (3)	
Center Luminance of White	L _C		(360)	(450)	-	cd/m ²	Note (4)	
White Variation	δW		-	-	(1.33)	-	Note (7)	
Cross Talk	CT		-	-	4	%	Note (5)	
Color Chromaticity	Red	$\theta_x = 0^\circ, \theta_y = 0^\circ$ Viewing angle at normal direction	(0.639)		-			
	Ry		(0.323)		-			
	Green		(0.305)		-			
	Gy		(0.625)		-			
	Blue		(0.144)		-			
	Bx		(0.065)		-			
	By		0.285		-			
	White		0.293		-			
Color Gamut			(72)	-	%	NTSC		
Viewing Angle	Horizontal	CR ≥ 20	80	88	-	Deg.	Note (1)	
			80	88	-			
	Vertical		80	88	-			
			80	88	-			

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80.

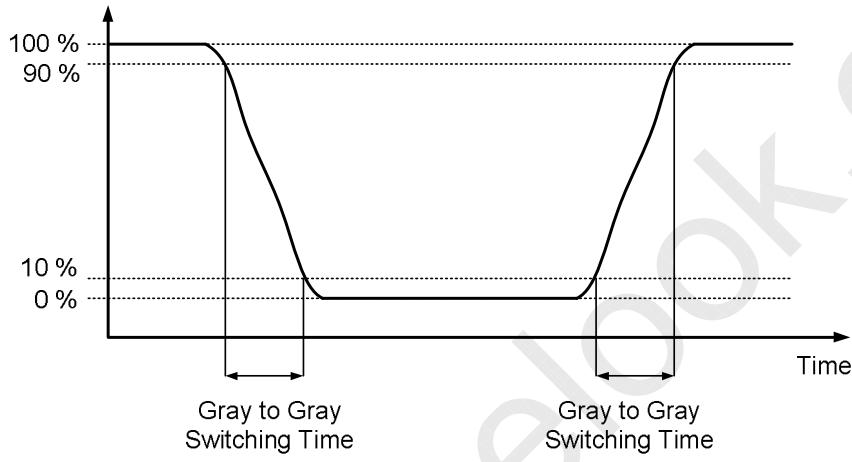


Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:**Optical Response**

The driving signal means the signal of gray level 0, 255, 511, 767, and 1023. Gray to gray average time means the average switching time of gray level 0, 255, 511, 767, 1023 to each other.

Note (4) Definition of Luminance of White (LC):

Measure the luminance of gray level 1023 at center point and 9 points

LC = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

Note (5) Definition of Cross Talk (CT):

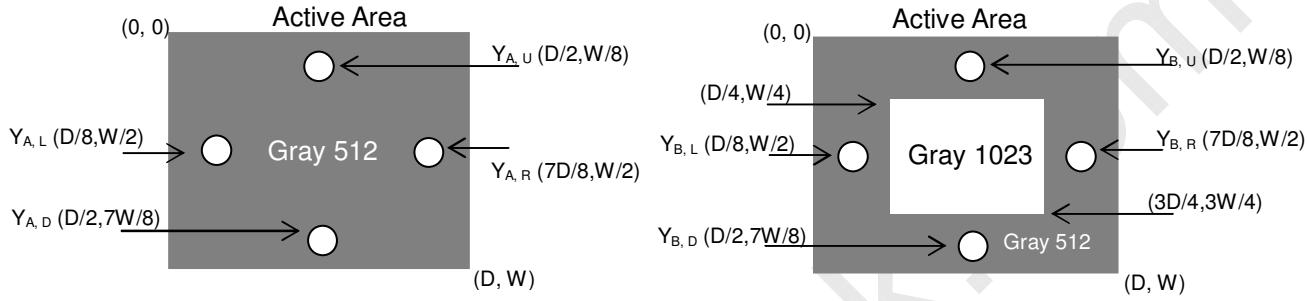
$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

(a)

Y_A = Luminance of measured location without gray level 1023 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 1023 pattern (cd/m^2)



(b)

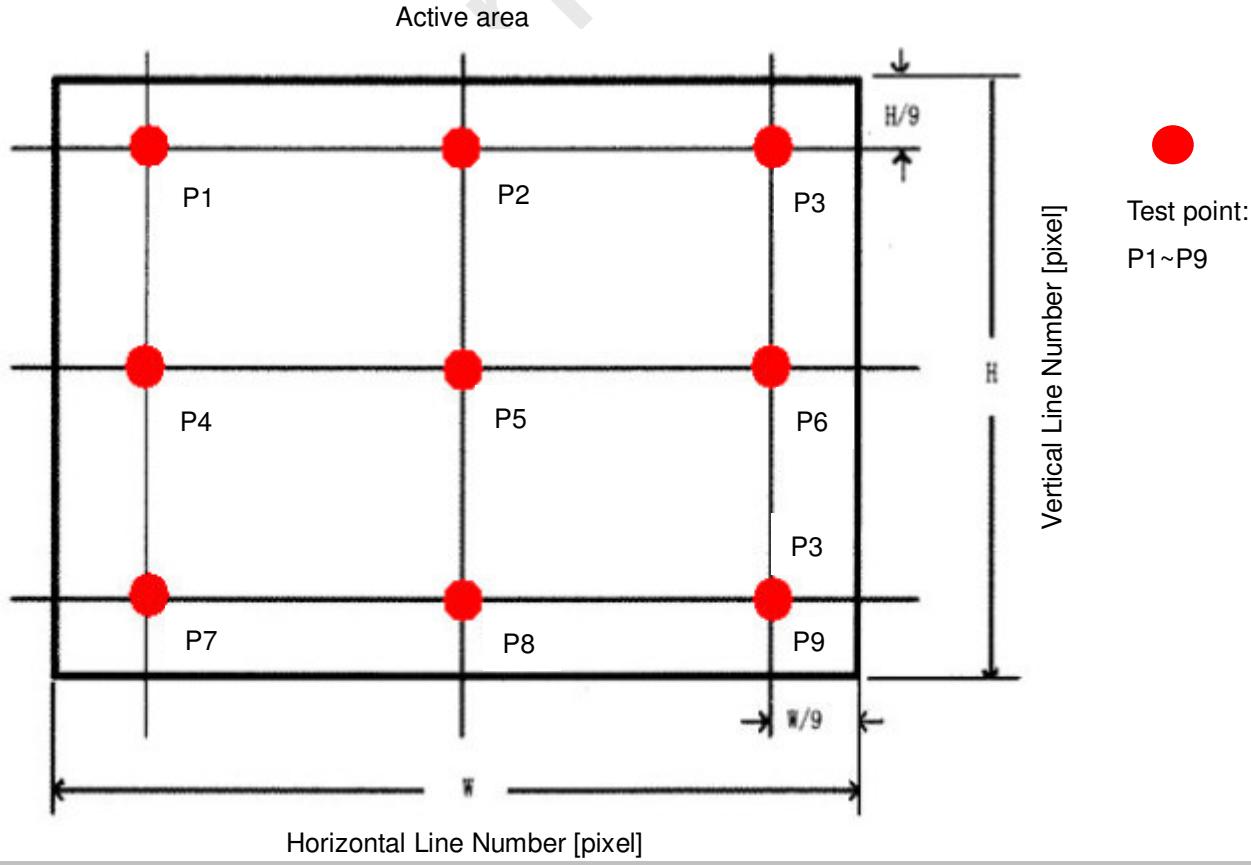
Y_A = Luminance of measured location without gray level 512 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 512 pattern (cd/m^2)

Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 9 points

δW = Maximum [L (1), L (2), L (3), ~ L (9)] / Minimum [L (1), L (2), L (3)~ L (9)]





PRODUCT SPECIFICATION

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [5] Do not plug in or pull out the I/F connector while the module is in operation.
- [6] Do not disassemble the module.
- [7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [8] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [9] When storing modules as spares for a long time, the following precaution is necessary.
 - [9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [10] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

- [1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [3] After the module's end of life, it is not harmful in case of normal operation and storage.

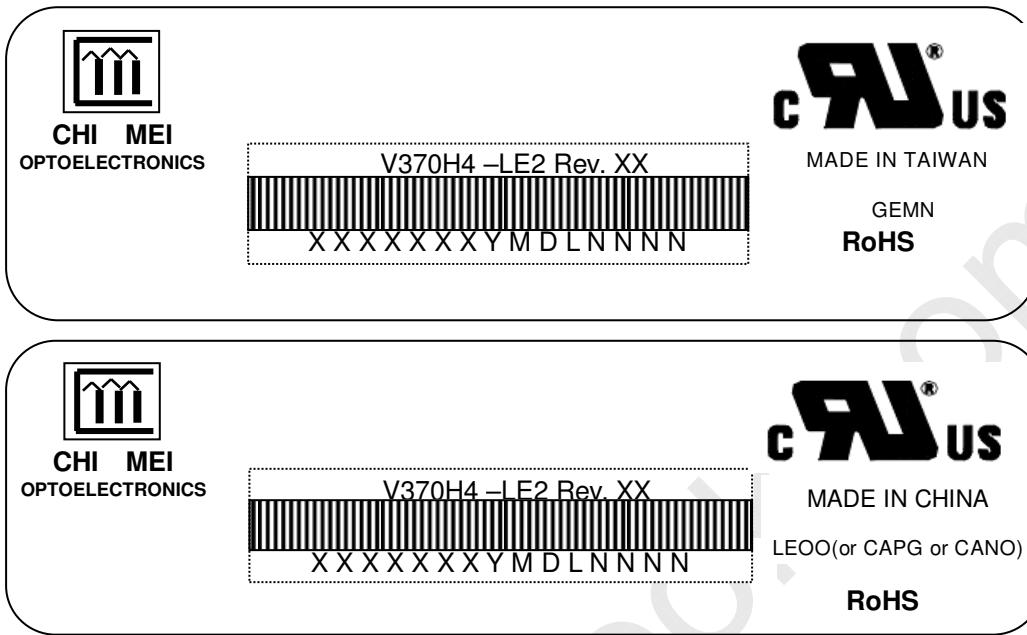


PRODUCT SPECIFICATION

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

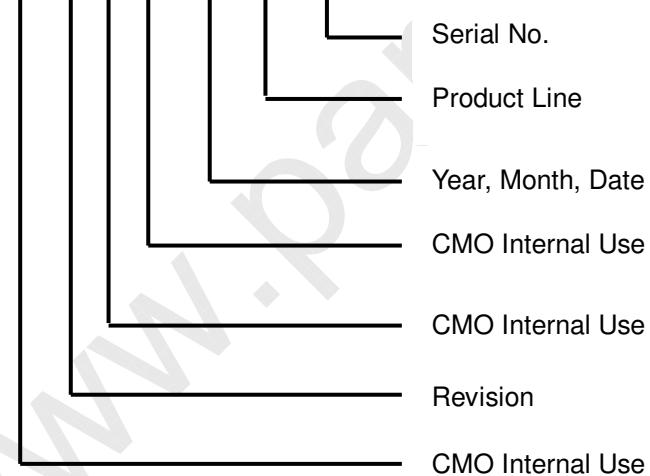
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V370H4-LE2

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: XX XXXX XXX Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 2001=1, 2002=2, 2003=3, 2004=4... 2010=0, 2011=1, 2012=2..

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

10. PACKAGING**10.1 PACKING SPECIFICATIONS**

- (1) 5 LCD TV modules / 1 Box
- (2) Box dimensions : 954(L)x283(W)x597(H)mm
- (3) Weight : approximately 34 Kg (5 modules per box)

10.2 PACKING METHOD

Figures 10.1 and 10.2 are the packing method

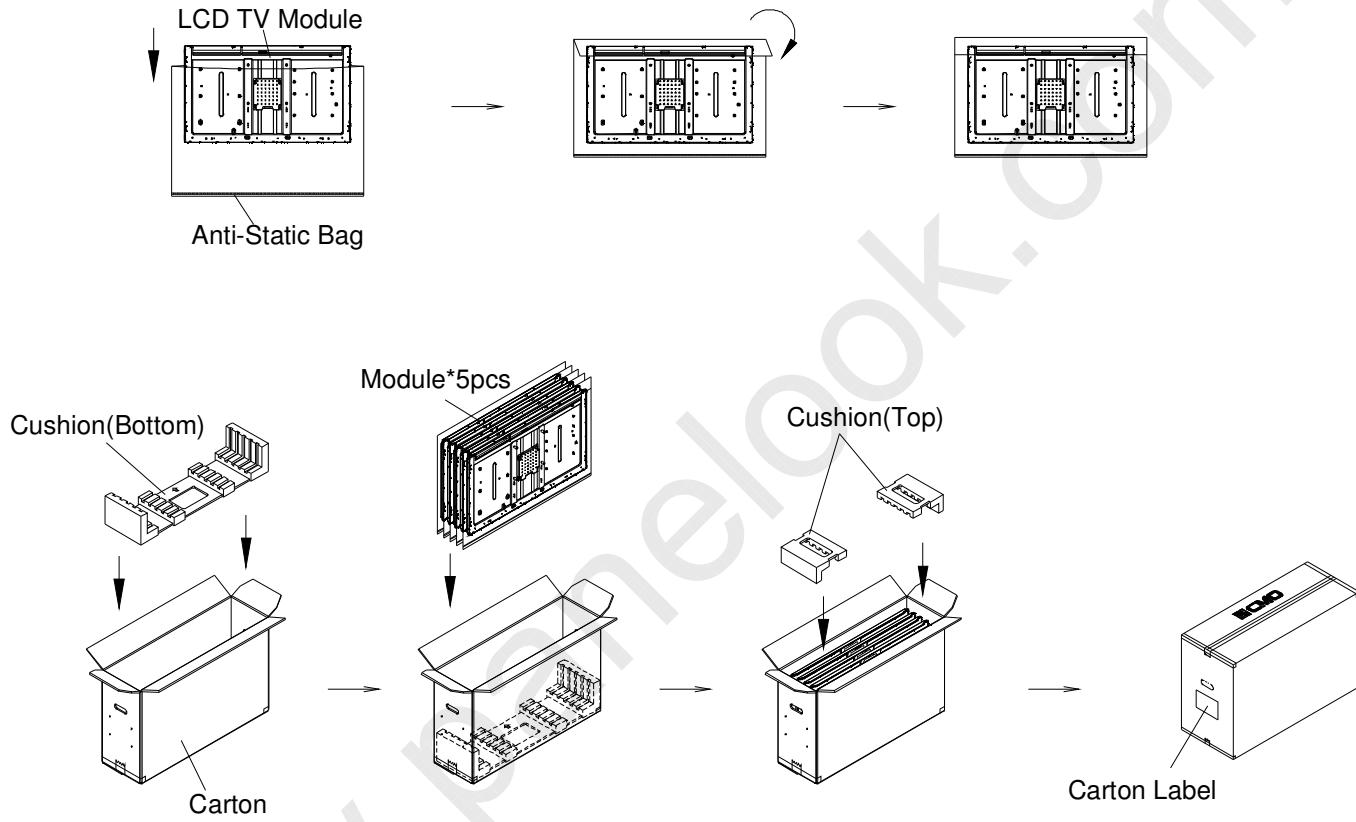
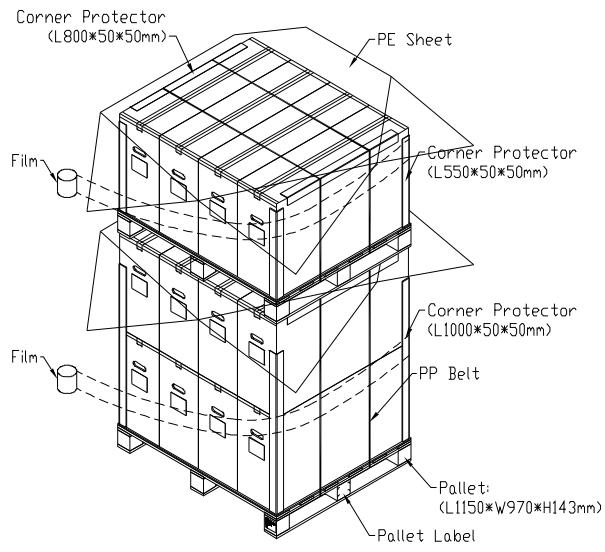
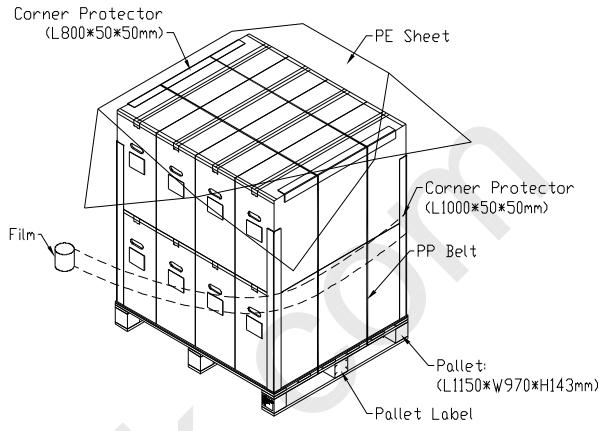


Figure.10.1 Packing method

**Sea / Land Transportation
(40ft HQ / 40ft Container)****Air Transportation****Figure.10.2 Packing method**

11. MECHANICAL CHARACTERISTICS
